WHAT IS CLAIMED IS:

1. A level shifter comprising:

a first transistor connected between a first power source line and an output node;

a second transistor connected between the output node and a second power source line;

a third transistor connected between the first power source line and the output node;

a fourth transistor connected between the output node and the second power source line; and

a control circuit that causes the second transistor and the fourth transistor to turn on when an input signal is of a first level and causes the third transistor and the first transistor to turn on when the input signal is of a second level different from the first level,

wherein a gate tolerant voltage of the first transistor is smaller than a gate tolerant voltage of the third transistor, and a gate tolerant voltage of the fourth transistor is smaller than a gate tolerant voltage of the second transistor.

2. A level shifter according to claim 1, wherein the control circuit comprises:

a fifth transistor which is connected between the first power source line and a first node, a gate thereof being connected with the output node;

a sixth transistor which is connected between the first node and the second power source line, in which a gate thereof receives the input signal;

a seventh transistor which is connected between the first power source line and a second node, in which a gate thereof receives the input signal; and

an eighth transistor which is connected between the second node and the second power source line, a gate thereof being connected with the output node.

3. A level shifter according to claim 2, wherein the control circuit further comprises an inverter circuit that produces an inverted input signal, a polarity of which being inverted, and supplies the inverted input signal to a gate of the second transistor and a gate of the third transistor.

4. A level shifter according to claim 2, wherein each of the first, fourth, fifth, and eighth transistors has a first gate tolerant voltage, and each of the second, third, sixth, and seventh transistors has a second gate tolerant voltage.

5. A level shifter according to claim 1, wherein each of the second and third transistors operates in a non-saturation region.

6. A level shifter according to claim 1, wherein the control circuit

causes the second transistor to turn on before turning on the fourth transistor when the input signal is of the first level and

causes the third transistor to turn on before turning on

the first transistor when the input signal is of the second level.

7. A level shifter according to claim 1, wherein a current supply capacity of the first transistor is larger than a current supply capacity of the third transistor and a current supply capacity of the fourth transistor is larger than a current supply capacity of the second transistor.

8. A level shifter according to claim 1, wherein the gate tolerant voltage of the first transistor and the gate tolerant voltage of the fourth transistor are equal to a voltage amplitude of an output signal outputted to the output node.

9. A level shifter according to claim 1, wherein the gate tolerant voltage of the second transistor and the gate tolerant voltage of the third transistor are equal to a voltage amplitude of an input signal.

10. A level shifter according to claim 2, wherein the first node and the second node are electrically connected with each other.

11. A level shifter according to claim 1, wherein the first transistor and the fourth transistor each are formed from a transistor that operates in a saturation region at a first speed and has a first current supply capacity, and the second transistor and the third transistor each are formed from a transistor that operates in a non-saturation region at a second speed lower than

the first speed and has a second current supply capacity lower than the first current supply capacity.

12. A level shifter comprising:

a first transistor of a first conductivity type having a first gate tolerant voltage, which is connected between a first power source line and a first node, in which a gate thereof receives an input signal;

a second transistor of a second conductivity type having a second gate tolerant voltage smaller than the first gate tolerant voltage, which is connected between a second power source line and a second node, in which a gate thereof is connected with the first node;

a third transistor of the first conductivity type having the first gate tolerant voltage, which is connected between the second node and the first power source line, in which a gate thereof receives an inverted input signal of the input signal;

a fourth transistor of the second conductivity type having the first gate tolerant voltage, which is connected between the second power source line and a third node, in which a gate thereof receives the input signal;

a fifth transistor of the second conductivity type having the second gate tolerant voltage, which is connected between the second power source line and the second node, in which a gate thereof receives the inverted input signal; and

a sixth transistor of the first conductivity type having the second gate tolerant voltage, which is connected between the second node and the first power source line, in which a gate

thereof is connected with the third node.

13. A level shifter according to claim 12, further comprising:

a seventh transistor of the second conductivity type having the second gate tolerant voltage, which is connected between the first node and the second power source line, in which a gate thereof is connected with the second node; and

an eighth transistor of the first conductivity type having the second gate tolerant voltage, which is connected between the third node and the first power source line, in which a gate thereof is connected with the second node.

14. A level shifter according to claim 13, wherein the first node and the third node are electrically connected with each other.

15. A level shifter comprising:

a first transistor of a first conductivity type, which is connected between a first power source line and a first node, in which a control terminal thereof is connected with a second node;

a second transistor of the first conductivity type, which is connected between the first power source line and the second node, in which a control terminal thereof is connected with the first node;

a third transistor of a second conductivity type, which is connected between the first node and a second power source

line, in which a control terminal thereof receives an input signal;

a fourth transistor of the second conductivity type, which is connected between the second node and the second power source line, in which a control terminal thereof receives an inverted input signal of the input signal;

a fifth transistor of the first conductivity type, which is connected between the first power source line and the second node, in which a control terminal thereof receives the inverted input signal;

a sixth transistor of the second conductivity type, which is connected between the second node and the second power source line, in which a control terminal thereof is connected with a third node;

a seventh transistor of the first conductivity type, which is connected between the first power source line and the third node, in which a control terminal thereof receives the input signal; and

an eighth transistor of the second conductivity type, which is connected between the third node and the second power source line, in which a control terminal thereof is connected with the second node,

wherein each of the first, second, sixth, and eighth transistors operates in a saturation region in accordance with a level of the input signal, and each of the third, fourth, fifth, and seventh transistors operates in a non-saturation region independently of the level of the input signal.